

REMARKS

Applicants request that the finality of the 12/20/05 Office Action be withdrawn. In this Office Action, "[c]laims 1-6 . . . are rejected under 35 U.S.C. 103(a) as being unpatentable over Annamalai . . . in combination with applicant's admitted prior art . . . and Temple . . . ."

The Temple patent was not used in the first Office Action to reject independent claims 1 and 3, and applicants did not amend claims 1 and 3 to require the use of the Temple patent. Therefore, because the rejection of these claims based on the newly cited Temple patent was not caused by applicants, the second Office Action should not have been made final.

Accordingly, applicants request that the finality of the 12/20/05 Office Action be withdrawn.

REJECTION

The Examiner rejected claims 1-6 and 32-35 under 35 U.S.C. §103(a) as being unpatentable over the Annamalai patent in view of admitted prior art and further in view of the Temple.

The Annamalai patent discloses a process for fabricating a silicon-on-diamond (SOD) structure

consisting of a silicon substrate, a thin film of deposited diamond on top of the silicon substrate, and an active silicon layer on top of the diamond film. Devices are fabricated in the active silicon layer. Diamond is used as an electrical insulator as compared with SOI, where silicon dioxide is used as an electrical insulator. The diamond film of the SOD structure has a high electrical resistivity and a high thermal conductivity.

As shown in Figure 1, two epitaxial layers 2 and 3 are grown on a seed silicon wafer 1. The layer 2 is an etch stop layer, and the layer 3 is an undoped silicon layer used to fabricate MOSFETs or bipolar transistors. A diamond layer 4 is deposited on top of the layer 3, a thin polysilicon layer 5 is deposited on top of the diamond layer 4, and a silicon handle wafer 6 is bonded on top of the polysilicon layer 5.

The seed silicon wafer 1 is then removed, and the etch stop layer 2 is removed. The resulting substrate, turned around, now consists of a silicon substrate 6, a polysilicon layer 5, a diamond layer 4, and an undoped silicon layer 3. Devices can be fabricated in the undoped silicon layer 3. This SOD structure now has a buried diamond layer with silicon on either side.

As shown in Figure 2, a SIMOX wafer 1-2-3 is the starting substrate. The buried oxide 2 is used as the etch stop layer, a diamond film 4 is deposited on top of the silicon layer 3, a thin polysilicon layer 5 is deposited on top of the diamond layer, and a silicon handle wafer 6 is now bonded to the thin polysilicon layer 5. The silicon layer 1 is removed, and the etch stop buried silicon dioxide layer 2 is removed. Devices can be fabricated in the thin silicon layer 3.

Figure 3 is used in the patent to show another process of making an SOD structure.

APPLICANTS' ARGUMENT

Independent claim 1 is directed to an RF semiconductor device comprising a high resistivity polysilicon handle wafer, a buried oxide layer over the polysilicon handle wafer, and a silicon layer over the buried oxide layer.

The Examiner appears to argue (i) that the Annamalai patent discloses the use of high resistivity polysilicon in fabricating semiconductor devices in general, (ii) that the present application discloses as "admitted prior art" the prior use of high resistivity GaAs in the fabrication of RF semiconductor devices, and

(iii) that the use of the semiconductor device disclosed in the Annamalai patent in RF applications is, therefore, suggested by the "admitted prior art" since both "references" rely on high resistivity materials. The Examiner then concludes on the basis of this suggestion that the use of the device disclosed in the Annamalai patent as an RF semiconductor device would have been obvious.

However, the Annamalai patent mentions nothing about the resistivity of the polysilicon layer 5 and does not disclose or suggest that the polysilicon layer 5 is a high resistivity polysilicon layer.

The Annamalai patent does state that the diamond layer 4 has a high resistivity on the order of  $10^{16}$  ohm-cm. However, independent claim 1 requires a high resistivity polysilicon handle wafer, not a high resistivity insulating layer.

Accordingly, since both "references" do not rely on high resistivity materials, there is no suggestion to use high resistivity polysilicon for the polysilicon disclosed in the Annamalai patent.

Similarly, as discussed below, the Temple patent does not disclose or suggest the use of high

resistivity polysilicon in the fabrication of semiconductor devices.

Therefore, there is no suggestion to combine the Annamalai patent, the "admitted prior art," and the Temple patent, and independent claim 1 is accordingly not unpatentable over the Annamalai patent in view of "admitted prior art."

EXAMINER'S REPLY

In the present Office Action, the Examiner asserts that the fact that the Annamalai patent fails to disclose a high resistivity polysilicon handle wafer is not relevant since the Examiner is relying only on the intermediate structure.

APPLICANTS' REBUTTAL

This assertion is rather cryptic in that the Examiner does not tell applicants the composition of the intermediate structure.

A first way to read the Examiner's assertion is that the Examiner is relying on the structure of Figure 1, 2, or 3 of the Annamalai patent as the intermediate structure since not one of these structures is the final structure, at least in the sense that the layers 1 and 2

must be removed to produce the final structure. However, even in this case, there is no disclosure in the Annamalai patent that the polysilicon layer 5 in any of these "intermediate" structures is high resistivity.

A second way to read the Examiner's assertion is that the Examiner is relying on the layers 3-6 as shown in Figure 1 or 2 or the layers 3-5 as shown in Figure 3 of the Annamalai patent as the intermediate structure, and that the final structure is one where the polysilicon layer is replaced by a high resistivity polysilicon layer. In this case, the Examiner must then be asserting that the use of high resistivity GaAs as disclosed in the "Admitted Prior Art" suggests to one of ordinary skill in the art the use of high resistivity polysilicon for the polysilicon shown in the Annamalai patent.

However, the combination of the "Admitted Prior Art" and the Annamalai patent can only at most suggest substituting high resistivity GaAs for the polysilicon shown in the Annamalai patent. There is no basis in either the Annamalai patent or the "admitted prior art" for suggesting to one of ordinary skill in the art the substitution of high resistivity polysilicon for the polysilicon disclosed in the Annamalai patent.

Moreover, as disclosed in the present application, the use of high resistivity silicon substrates in RF applications was known to be problematical because donors that are thermally generated during post-processing degrade the resistivity both at the SiO<sub>2</sub>/Si interface. This degradation produces higher losses, increases coupling (cross-talk), lowers inductor Q, and is not so easily remedied. Therefore, one of ordinary skill in the art would not have looked to silicon as a solution to this degradation problem and instead would have used GaAs.

Accordingly, for both of these reasons, the Annamalai patent and the "Admitted Prior Art" would not have suggested to one of ordinary skill in the art the use high resistivity polysilicon to produce the invention of independent claim 1.

The Temple patent, relied by the Examiner in the rejection of independent claim 1, discloses a semiconductor package 10 for a semiconductor chip 12. The semiconductor package 10 has a high resistivity polysilicon base 15, a high resistivity polysilicon sidewall 20, and a high resistivity polysilicon cover 30. The high resistivity polysilicon base 15 centrally supports the semiconductor chip 12, and an exposed

peripheral surface 16 of the base 15 engages the high resistivity polysilicon sidewall 20. An upper surface 22 of the high resistivity polysilicon sidewall 20 engages a lower surface 28 of the high resistivity polysilicon cover 30.

The high resistivity polysilicon cover 30 includes external terminals 31 and a means to couple a signal between the external terminals 31 and electrodes 13 of the semiconductor chip 12. This means includes a highly conductive region 32 of the high resistivity polysilicon cover 30, a contact washer 25, and a metal 27.

There is no disclosure in the Temple patent that high resistivity polysilicon is used in the fabrication of the semiconductor chip 12, only in the packaging 10 for the semiconductor chip 12. Accordingly, the Temple patent does not suggest to one of ordinary skill in the art fabricating the semiconductor chip disclosed in the Annamalai patent with high resistivity polysilicon.

Consequently, the combination of the Annamalai patent, the "admitted prior art," and the Temple patent would not have suggested to one of ordinary skill in the art the fabrication of a semiconductor chip with high

resistivity polysilicon. Therefore, independent claim 1 is not unpatentable over the Annamalai patent in view of "admitted prior art" and further in view of the Temple.

Independent claim 3 is directed to an RF semiconductor device comprising a high resistivity polycrystalline layer, a buried oxide layer over the polycrystalline layer, and a silicon layer over the buried oxide layer.

The Examiner appears to argue (i) that the Annamalai patent discloses the use of high resistivity polycrystalline in fabricating semiconductor devices in general, (ii) that the present application discloses as "admitted prior art" the prior use of high resistivity GaAs in the fabrication of RF semiconductor devices, and (iii) that the use of the semiconductor device disclosed in the Annamalai patent in RF applications is, therefore, suggested by the "admitted prior art" since both "references" rely on high resistivity materials. The Examiner then concludes on the basis of this suggestion that the use of the device disclosed in the Annamalai patent as an RF semiconductor device would have been obvious.

However, the Annamalai patent mentions nothing about the resistivity of the polysilicon layer 5 and does not disclose or suggest that the polysilicon layer 5 is a high resistivity polysilicon layer.

The Annamalai patent does state that the diamond layer 4 has a high resistivity on the order of  $10^{16}$  ohm-cm. However, independent claim 3 requires a high resistivity polycrystalline handle wafer, not a high resistivity insulating layer.

Accordingly, since both "references" do not rely on high resistivity materials, there is no suggestion to use high resistivity polycrystalline for the polysilicon disclosed in the Annamalai patent.

Similarly, as discussed below, the Temple patent does not disclose or suggest the use of high resistivity polycrystalline in the fabrication of semiconductor devices.

Therefore, there is no suggestion to combine the Annamalai patent, the "admitted prior art," and the Temple patent, and independent claim 3 is accordingly not unpatentable over the Annamalai patent in view of "admitted prior art."

EXAMINER'S REPLY

In the present Office Action, the Examiner asserts that the fact that the Annamalai patent fails to disclose a high resistivity polysilicon handle wafer is not relevant since the Examiner is relying only on the intermediate structure.

APPLICANTS' REBUTTAL

This assertion is rather cryptic in that the Examiner does not tell applicants the composition of the intermediate structure.

A first way to read the Examiner's assertion is that the Examiner is relying on the structure of Figure 1, 2, or 3 of the Annamalai patent as the intermediate structure since not one of these structures is the final structure, at least in the sense that the layers 1 and 2 are removed to produce the final structure. However, even in this case, there is no disclosure in the Annamalai patent that the polysilicon layer 5 in any of these "intermediate" structures is high resistivity.

A second way to read the Examiner's assertion is that the Examiner is relying on the layers 3-6 as shown in Figure 1 or 2 or the layers 3-5 as shown in Figure 3 of the Annamalai patent as the intermediate

structure, and that the final structure is one where the polysilicon layer is replaced by a high resistivity polysilicon layer. In this case, the Examiner must then be asserting that the use of high resistivity GaAs as disclosed in the "Admitted Prior Art" suggests the use of high resistivity polysilicon for the polysilicon shown in the Annamalai patent.

However, the combination of the "Admitted Prior Art" and the Annamalai patent can only at most suggest substituting high resistivity GaAs for the polysilicon shown in the Annamalai patent. There is no basis in either the Annamalai patent or the "admitted prior art" for suggesting to one of ordinary skill in the art the substitution of high resistivity polysilicon for the polysilicon disclosed in the Annamalai patent.

Moreover, as disclosed in the present application, the use of high resistivity silicon substrates in RF applications was known to be problematical because donors that are thermally generated during post-processing degrade the resistivity both at the SiO<sub>2</sub>/Si interface. This degradation produces higher losses, increases coupling (cross-talk), lowers inductor Q, and is not so easily remedied. Therefore, one of ordinary skill in the art would not have looked to

silicon as a solution to this degradation problem and instead would have used GaAs.

Accordingly, for both of these reasons, the Annamalai patent and the "Admitted Prior Art" would not have suggested to one of ordinary skill in the art the use high resistivity polycrystalline to produce the invention of independent claim 3.

As discussed above, there is no disclosure in the Temple patent that high resistivity polycrystalline is used in the fabrication of the semiconductor chip 12. Accordingly, the Temple patent does not suggest to one of ordinary skill in the art fabricating the semiconductor chip disclosed in the Annamalai patent with high resistivity polycrystalline.

Consequently, the combination of the Annamalai patent, the "admitted prior art," and the Temple patent would not have suggested to one of ordinary skill in the art the fabrication of a semiconductor chip with high resistivity polycrystalline. Therefore, independent claim 3 is not unpatentable over the Annamalai patent in view of admitted prior art and further in view of the Temple.

Because independent claims 1 and 3 are not unpatentable over the Annamalai patent in view of

admitted prior art and further in view of the Temple, dependent claims 2 and 4-6 are likewise not unpatentable over the Annamalai patent in view of admitted prior art and further in view of the Temple.

Dependent claims 32 and 34 recite that the high resistivity polysilicon or polycrystalline handle wafer comprises a high resistivity polysilicon or polycrystalline handle wafer having a resistivity  $\rho$  greater than  $10^6 \Omega\text{-cm}$ . The art applied by the Examiner does not show a polysilicon or polycrystalline handle wafer having this resistivity.

Moreover, the Temple patent discloses the use of high resistivity polysilicon in packaging a chip but does not disclose or suggest the use of high resistivity polysilicon in the fabrication of the chip itself. Therefore, the Temple patent cannot suggest the invention of dependent claims 32 and 34 to one of ordinary skill in the art.

Accordingly, dependent claims 32 and 34 are patentable over the Annamalai patent in view of "admitted prior art" and further in view of the Temple patent.

Dependent claims 33 and 35 recite that the silicon layer comprises an RF processed silicon layer.

The art applied by the Examiner does not show an RF processed silicon layer.

The Examiner gives no weight to a limitation of a claim, thereby conveniently ignoring a limitation for which the Examiner has cited no art. It is improper to ignore limitations that an Examiner cannot find in the prior art.

Accordingly, dependent claims 33 and 35 are patentable over the Annamalai patent in view of admitted prior art and further in view of the Temple patent.

CONCLUSION

In view of the above, it is clear that the claims of the present application are patentable over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the above captioned patent application are respectfully requested.

Respectfully submitted,

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